ABSTRACT OF THE DISCLOSURE

The invention relates to an integrated circuit of reduced parasitic capacitive influences and to a method of its fabrication. It is an object of the invention to propose an integrated circuit of reduced parasitic capacitive influences and a method of its fabrication in which the parasitic capacitive influences for individual especially passive elements of the integrated circuit is reduced. In addition, the technological sequence for realizing the contact and conductor system of modern CMOS or CMOS compatible silicon technologies is not to be adversely affected during the fabrication of circuits with integrated passive elements and, in particular, no additional planarizing steps are to become necessary. The object is accomplished by an at least partial insulating layer of a thickness of at least 5 μm which is locally restricted to the area of the elements of the integrated circuit and which is buried in the semiconductor substrate. The losses caused by parasitic influences and dependent upon the specific electrical resistance of the silicon substrate used, are significantly reduced so that depending upon the selected thickness of the buried insulating layer, the quality of an integrated inductance may be improved by about 40 % or more relative to planar inductances based upon conventional CMOS.